PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference WK04-042-PCT	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/JP2004/016792	International filing date *(day/month/year)* 05.11.2004	Priority date *(day/month/year)* 12.11.2003
International Patent Classification (IPC) or national classification and IPC H01L29/739, H01L29/78, H01L29/423		
Applicant TOYOTA JIDOSHA KABUSHIKI KAISHA et al.		

1. This report is the International preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 4 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 2 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
16.08.2005	25.01.2006
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized Officer Baillet, B Telephone No. +31 70 340-3379

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/016792

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-17	as originally filed
Claims, Numbers	
1-6	received on 16.08.2005 with letter of 11.08.2005
Drawings, Sheets	
1/7-7/7	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2,6
	No:	Claims	1,3-5
Inventive step (IS)	Yes:	Claims	2,6
	No:	Claims	1,3-5
Industrial applicability (IA)	Yes:	Claims	1-6
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following document :

D2: PATENT ABSTRACTS OF JAPAN vol. 2000, no. 05, 14 September 2000 (2000-09-14) & JP 2000 058823 A (TOSHIBA CORP), 25 February 2000 (2000-02-25)

1. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1 and 3-5 is not new in the sense of Article 33(2) PCT.

1.1 The document D2 discloses (the references in parentheses applying to this document, see in particular figure 3) a semiconductor device which can be an IGBT (see D2, paragraph [0022]) comprising a top region (5) of a second conductivity type, a deep region (2) of the second conductivity type, an intermediate region (3) of a first conductivity type isolating the top region (5) from the deep region (2), an emitter electrode (10) connected with the top region, a collector region of a first conductivity type contacting the deep region (2) and being isolated from the intermediate region (3) by the deep region and a collector electrode, which are implicitly present in the case where the device disclosed in D2 is an IGBT, and a trench gate (8) facing a portion of the intermediate region (3) via an insulating region (7), the portion facing the trench gate (8) isolating the top region (5) and the deep region (2), the trench gate (8) extending along a longitudinal direction with its width varying along this longitudinal direction (see D2, figure 3). Hence the subject-matter of claim 1 is not new (Article 33(2) PCT).

1.2 The subject-matter of dependant claims 3-5 is also disclosed in D2 (see D2, figure 3). Hence the subject-matter of claims 3-5 is not new (Article 33(2) PCT).

2. The combination of the features of dependent claims 2 and 6 is neither known from, nor rendered obvious by, the available prior art. The variation in phase of the width of adjacent trench gates to allow that the region between two wide parts of adjacent trench gates becomes depressed when a no on-voltage is applied to the trench gates, is made to restrict the pathway of minority carriers in the intermediate region. This problem is not the same which is solved by the device disclosed in D2.

Amendments under Article 34(2)b of PCT

CLAIMS

1. A semiconductor device of IGBT comprising:

a top region of a second conductivity type;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type for isolating the top region and the deep region;

a collector region of the first conductivity type contacting with the deep region and being isolated from the intermediate region by the deep region;

an emitter electrode connected with the top region;

a collector electrode connected with the collector region; and

a trench gate facing a portion of the intermediate region via an insulating layer, wherein the portion facing the trench gate isolates the top region and the deep region, and wherein the trench gate extends along a longitudinal direction and width of the trench gate varies along the longitudinal direction.

2. A semiconductor device according to claim 1,

wherein a plurality of trench gates extending in parallel is provided, and variations of width of trench gates along the longitudinal direction are aligned in phase between adjacent trench gates.

3. A semiconductor device according to any of the preceding claims,

wherein a side wall of the trench gate at a wider width is parallel with a side wall of an adjacent trench gate.

4. A semiconductor device according to any of the preceding claims,

wherein a pair comprising a wide trench gate and a narrow trench gate is repeated along the longitudinal direction, and total length of the wide trench gates is 30 to 80 % of the total length of the trench gate.

5. A semiconductor device according to any of the preceding claims, wherein variations of width of each trench gate along the longitudinal direction are repeated cyclically along the longitudinal direction.

6. A semiconductor device according to any of the preceding claims, wherein width of the intermediate region interposed between adjacent wide trench gates is narrow such that the intermediate region interposed between adjacent wide trench gates becomes a depressed region when on-voltage is not being applied to the trench gates, and the top region is located above the intermediate region interposed between adjacent wide trench gates.